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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/062,047
	Filing Date	1/31/02
	First Named Inventor	Steven Teig, et al.
	Group Art Unit	2825
	Examiner Name	B. Tat
Total Number of Pages in This Submission	Attorney Docket Number	SPLX.P0101

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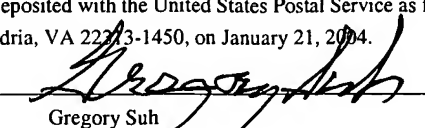
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PATENT
Docket No. SPLX.P0101

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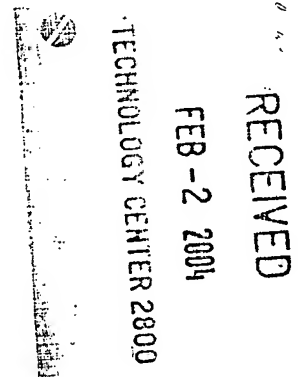
In the application of:

Steven Teig, et al.

Serial No.: 10/062,047

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
PERFORMING TECHNOLOGY
MAPPING



INFORMATION DISCLOSURE
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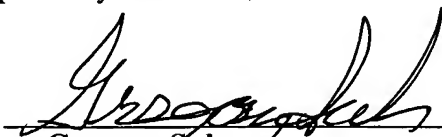
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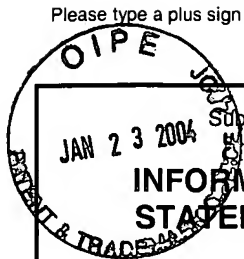
Dated: January 21, 2004

Respectfully submitted,

By: 
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/062,047
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
Sheet	1	of	3	Attorney Docket Number	SPLX.P0101

U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	U.S. Patent Document Number Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	2002/01570 63	A1	10-24-2002	Besson
	2.	2002/01784 32	A1	11-28-2002	Kim et al.
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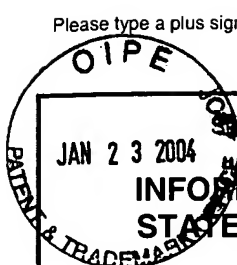
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
Sheet	2	of	3	Attorney Docket Number	SPLX.P0101

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	43.	6,574,779	B2	06-03-2003	Allen et al.	

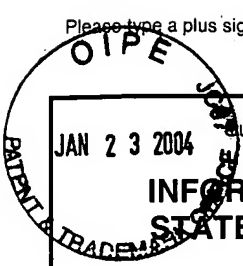
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				Group Art Unit	2825
				Examiner Name	B. Tat
Sheet	3	of	3	Attorney Docket Number	SPLX.P0101

U.S. PATENT DOCUMENTS

44.	6,618,835	B1	09-09-2003	Garlapati et al.
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NON PATENT LITERATURE DOCUMENTS

Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	45.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).	
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	48.	Devadas, S. et al., Synthesis and Optimization for Robustly Delay-fault Testable Combinational Logic Circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp.221-227.	
	49.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.	
	50.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.	
	51.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.	
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